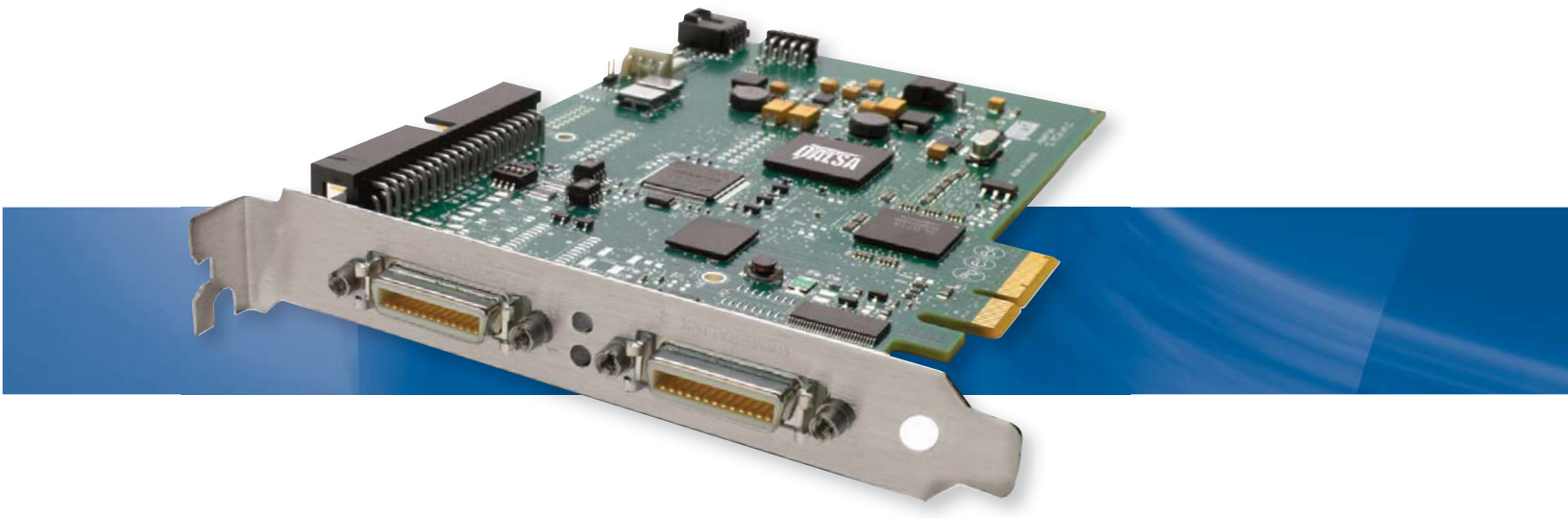
X64 Xcelera-CL PX4 SE

Embedded Processing Frame Grabber with PCI Express x4 Interface

Building on the field proven technology of DALSA's X64 Xcelera frame grabbers, the new X64 Xcelera-CL PX4 Special Edition (SE) board leverages the PCI Express (PCIe) platform to combine traditional image acquisition with embedded processing functions to enhance system performance and flexibility.



Key Features

- Half-length PCIe x4 Board
- Supports area or line scan Base, Medium or Full Camera Link® cameras
- Supports Power-Over-Camera Link for Base Cameras
- On-board image pre-processing functions
  - Multi-threshold real-time RLE
  - Color space conversion
  - Dynamic multiple LUTs
  - Dynamic multiple FFC/FLC
  - Concurrent multiple output streams for raw and processed images
- Rapid image acquisition rates up to 1GB/s and high-speed image transfer to host memory at 1GB/s
- Windows Vista and XP Professional compatible (32/64-bit)
- ROHS compliant

The X64 Xcelera-CL PX4 SE offers real-time image processing functions such as Run-length Encoding (RLE), color space conversion for Bayer, RGB and CIELAB, multiple dynamically switchable lookup tables and support for multiple shading correction configuration sets.

Advanced PCIe x4 image acquisition and processing

The PCIe host interface is a point-to-point interface that facilitates simultaneous image acquisition and transfer without loading the system bus or requiring significant intervention from the host CPU. The X64 Xcelera-CL PX4 SE is a Camera Link frame grabber that uses a PCI Express x4 interface. Compatible with a Base, Medium or Full Camera Link camera, the X64 Xcelera-CL PX4 SE board supports a wide variety of multi-tap area and line scan color and monochrome cameras. For greater versatility, X64 Xcelera-CL PX4 SE can be interfaced with custom camera pixel depths and tap configurations such as 10-taps cameras.

Designed with the requirements of machine vision OEMs in mind, the Xcelera Series of products deliver bandwidth of 1GB/sec over multiple-lane PCI Express implementations with room to grow.

Run-Length Encoding

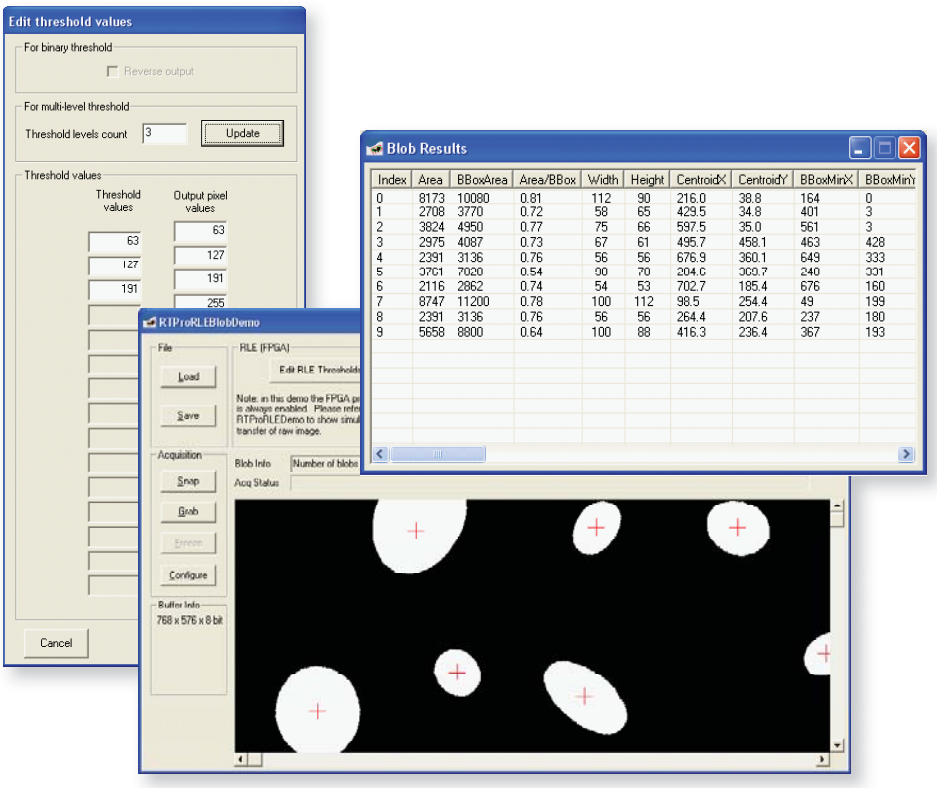
Run-Length Encoding (RLE) is a technique widely used to perform blob analysis operations, to detect defects or to classify objects. This technique is also used in image processing applications to reduce raw input data. X64 Xcelera-CL PX4 SE features 32 level thresholding and dual-destination output streams when performing run-length encoding functions. It is, therefore, possible to transfer the input image and the processed data simultaneously to the host computer for subsequent processing.

The RLE output format from the X64 Xcelera-CL PX4 SE is fully compatible with DALSA's Sapera Essential Blob-Analysis tool and can be combined to increase the processing speed.

The board's hardware assisted run-length encoding functions support 8, 10 or 12-bit area or line scan cameras in Base, Medium or Full Camera Link configurations.

TRIGGER-TO-IMAGE RELIABILITY

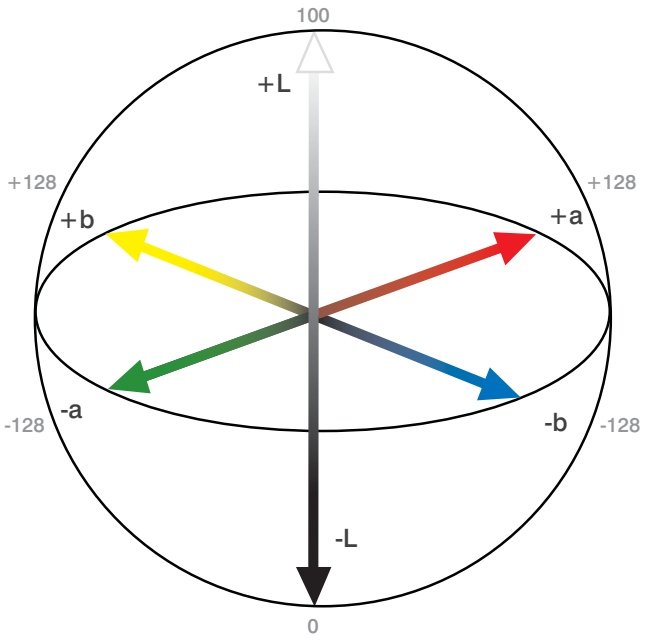
Xcelera-CL PX4 SE board is built within DALSA's Trigger-to-Image Reliability technology framework. Trigger-to-Image Reliability leverages DALSA's hardware and software innovations to control, monitor and correct the image acquisition process from the time that an external trigger event occurs to the moment the data is sent to the host, providing traceability when errors do occur and permitting recovery from those errors.



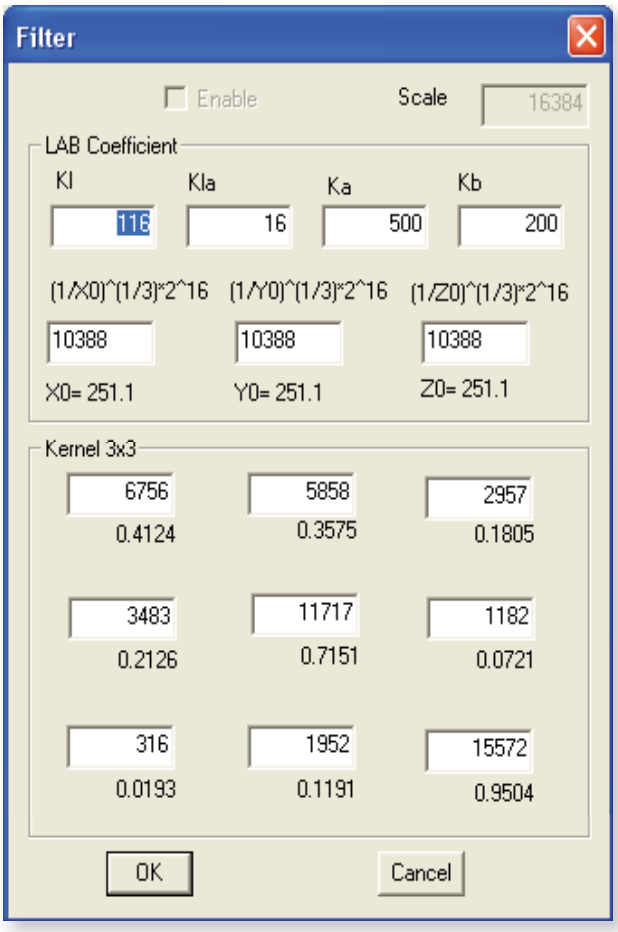
Run-Length Encoding

Color Space Converter

The X64 Xcelera-CL PX4 SE offers real-time color space conversion for the L*a*b color space, including RGB to CIELAB, Bayer to CIELAB [1], and Bayer to RGB color conversion capabilities. The CIELAB (L*a*b*) algorithm represents the most perceptually linear color space. By removing the affects of luminance, the color representation is perceptually more precise allowing color segmentation to be more perceptually accurate than any other color space technique. This compute-intense algorithm supports 8, 10 and 12-bit color pixel formats.



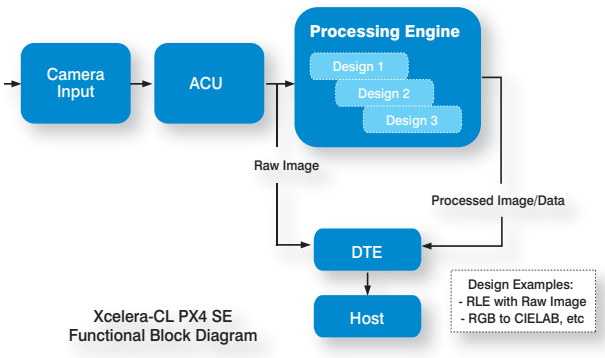
*L*a*b color space*



Color Space Converter

Dual Destination Transfers

The X64 Xcelera-CL PX4 SE is capable of transferring raw, processed and converted images simultaneously to the host memory. The transferred images can be sent to independent image destination buffers to avoid unnecessary copying operations. The PCIe bandwidth is exploited to its fullest by combining multiple pixel formats in one transfer operation. User applications benefit from having data in ready-to-use packed or planar formats while having access to the original image intact, making the best use of available resources.



Xcelera-CL PX4 SE
Functional Block Diagram

Dynamic Look-Up-Tables (LUTs)

The X64 Xcelera-CL PX4 SE supports multiple input lookup tables that, once loaded, can be switched dynamically while grabbing images. Dynamic LUTs are useful in applications where the sequence of images being acquired requires different thresholds due to varying lighting angles and sources.

Multi-FFC/FLC

Similar to Dynamic LUTs, the X64 Xcelera-CL PX4 SE offers a multiple Flat-Field Correction and Flat-Line Correction (FFC/FLC) feature. The multi-FFC/FLC can be used in applications where gain and offset parameters require modifications due to extreme thermal, line rate, exposure time, or direction variation. The calibration sets can be generated ahead of time for different operating conditions and utilized at run-time without stopping production lines.

Software Support

The X64 Xcelera-CL PX4 SE is supported by a feature rich software package including: Sapera Essential, board level image acquisition and control libraries and advanced embedded processing functions for RLE, color space conversion, dynamic LUT and multi-FFC/FLC capabilities; plus extensive example applications, documentation and application source code. This advanced software library supports Windows XP Professional and Windows Vista (32/64-bit). Applications can be developed using Microsoft Visual C/C++ 6.0 or higher in 32 bit environment and Microsoft Visual Studio 2005 or above in 64-bit environment.

[1] Contact DALSA Sales for Availability

Specifications*

Function	Description
Board	Camera Link Specifications Rev. 1.1 compliant Half length PCI Express 1.1 x4 compliant ROHS Compliant Supports PoCL
Acquisition	Supports one Base, Medium or Full Camera Link area or line scan camera Acquisition pixel clock rates up to 85MHz
Resolution	Horizontal Size (min/max): 8 byte/256K bytes Vertical Size (min/max): 1 line/infinite lines for line-scan cameras 1 line/16million lines/frame for area-scan cameras Variable length frame size from 1 to 16 million lines for area or line scan cameras 128MB onboard frame buffer memory Integrated advanced tap reversal engine allows independent tap formatting
Pixel Format and Tap configurations	Supports Camera Link tap configurations for 8, 10, or 12-bit mono and RGB For Base cameras in any of the following combinations: 3x8-bit/tap, 2x10-bits/tap, 2x12-bit/tap, 1x14-bit/tap, 1x16-bits/tap, & 1x24-bit/RGB For Medium camera - 4x8-bit/tap, 4x10-bits/tap, 4x12-bit/tap, 1x30-bit/RGB, & 1x36-bits/tap For Full – 8x 8-bit/tap CameraLink ; 10x8-bit non-Camera Link configuration
Transfers	Real-time transfers to system memory Intelligent Data-Transfer-Engine automatically loads scatter-gather and tap description tables from the host memory without CPU intervention
On-board Processing	
Bayer Mosaic Filter	Hardware Bayer Engine supports one 8, 10 or 12-bit Bayer camera input Bayer output format supports 8 or 10-bit RGB/pixel Supports Camera Link Base Camera Link cameras Zero host CPU utilization for Bayer conversion
Bayer to L*a*b Converter [1]	Hardware Bayer engine supports 8, 10 or 12-bit Bayer cameras Output format supports 8, 10 or 12 L*a*b with raw Bayer output in 8, 10 or 12-bit/pixel Supports Camera Link Base Link cameras Planar or packed data formats Zero host CPU utilization for Bayer conversion
Shading Correction	On the fly flat-line and flat-field correction with dead-pixel replacement Supports Camera Link Base, Medium or Full cameras User programmable calibration gain/offset maps Up to 16 calibration sets can be loaded on the board

Function	Description
RLE	Max Image Size: 8k x 64k Max Taps: 8-bit/8 taps Pixel Format: 8, 10, 12, 14 and 16-bit/pixel Max Number of threshold: 32
Output Lookup Tables	Supports up to 16 lookup tables simultaneously in Monochrome: 256x8-bit, 1024x10-bit, 1024x8-bit, 4096x12-bit, 4096x10-bit or 4096x8-bit
Color	8-bit in/out, 10-bit in 8 or 10-bit out, 12-bit in 12, 10 or 8-bit/out Lookup table
Controls	Comprehensive event notification includes end/start-of-field/frame/transfer Camera control signals for external event synchronization Optically isolated TTL/LVDS trigger input programmable as active high or low (edge or level trigger) TTL Strobes output PC independent serial communications ports provide support 9600 to 11500K baud Appear as system serial ports enabling seamless interface to host applications
Shaft-Encoder Input	Optically isolated quadrature (AB) shaft-encoder inputs for external web synchronization Supports up/down scaling
On-board I/Os [2]	4-optically isolated general purpose inputs support 5V and 24V DC signals, switch selectable 4 general purpose outputs
Power Output	Power-on-reset fused +12V output @ 1.5A +5V DC output at 1.5A
Software	Device driver supports : Microsoft Windows XP/VISTA compliant Supports Microsoft Windows VISTA 64-bit Full support of DALSA's Sapera Essential, Sapera LT and Sapera Processing software libraries Application development using C++ DLLs and ActiveX controls with Microsoft Visual Studio
System Requirements	PCI Express 1.1 or higher compliant with one x4 slot system with 64MB or higher system memory
Dimensions	6.375" (16.2cm) Length X 4.20" (10.7cm) Height)
Temperature	0°C (32° F) to 55° C (131° F) Relative Humidity: up to 95% (non-condensing)
Markings	FCC Class B – Approved CE – Approved

* Specifications can be changed without prior notice

[1] Contact DALSA Sales for Availability

[2] Requires a separate slot for the bracket assembly

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DALSA is an international leader in digital imaging and semiconductors and has its corporate offices in Waterloo, Ontario, Canada.